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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,580	04/13/2001	Joel Zvi Apisdorf	ACRN-003/00US	5628

26384 7590 05/21/2004

NAVAL RESEARCH LABORATORY
ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
4555 OVERLOOK AVENUE, S.W.
WASHINGTON, DC 20375-5320

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	8

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,580	APISDORF ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/23/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-30* is/are allowed.

6)☒ Claim(s) *1-14, and 19-23* is/are rejected.

7)☒ Claim(s) *15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 11, and 15-22 are objected to because of the following informalities:

in claim 11, line 2, "is" should read --are--. Appropriate correction is required;

in claim 15, line 3, "determining that" is confusing. It is suggested to change "that" to --whether--;

in claim 17, line 3, "determining that" is confusing. It is suggested to change "that" to --whether--;

in claim 19, line 3, "determining that" is confusing. It is suggested to change "that" to --whether--; and

in claim 22, line 3, "determining that" is confusing. It is suggested to change "that" to --whether--.

Claim Rejections - 35 USC § 112

2. Claims 11, and 19-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, "said first processing element" and "said second processing element" lack proper antecedent basis since they were not defined previously.

In claim 19, line 3, it is not clear what is meant by "determining that the first instruction identifies a second thread" since the term of "identifies" was not defined previously. In combination with the objection set forth above, it is suggested to change "determining that the first instruction identifies a second thread" to -- determining whether a second thread depends on the first instruction--; and similarly in lines 4-5, change "said first instruction identifies the second thread" to -- the second thread depends on said first instruction--.

In claim 22, line 3, it is not clear what is meant by "determining the first instruction identifies a second thread" since the term of "identifies" was not defined previously. In combination with the objection set forth above, it is suggested to change "determining the first instruction identifies a second

thread" to -- determining whether a second thread depends on the first instruction--.

In claim 22, line 5, it is not clear what is meant by "examining indicates a non-zero value" since the relationship between "a non-zero value" and the other elements was not defined previously. Should "a non-zero value" change to -the counter comprising a non-zero value-- ?

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-14, and 23 are rejected under 35 U.S.C. 102(a) as being anticipated by Akkary et al. (U.S. Patent No. 6,182,210) hereafter referred to as Akkary et al.

Referring to claim 1, Akkary et al. discloses as claimed an apparatus for instruction-level parallelism in a processing element, comprising: an instruction control unit (control circuitry 224A, see Fig. 10); a first instruction buffer (instruction queue array 202A, see Fig. 10) coupled to said instruction control unit (control circuitry 224A, see Fig. 10); a second instruction buffer (instruction queue array 202A, see Fig. 10, see also col. 9, lines 48-52, regarding instructions are written into different trace buffer (comprising different instruction queue array 202A therein) or into instruction queue array 202A at a different time) coupled to said instruction control unit; a dependency counter (data and dependency array 206A see Fig. 10, and see also col. 10, lines 58-67, and col. 11, lines 1-34) coupled to said instruction control unit; an execution switch (SCHED/ISSUE 156, see Fig. 2) coupled to (best reasonably and broadly interpreted, see Fig. 2) said instruction control unit (control circuitry 224A, see Fig. 10), said first instruction buffer (instruction queue array 202A, see Fig. 10), and said second instruction buffer (instruction queue array 202A, see Fig. 10); and an execution unit (EXEC UNITS 158, see Fig. 2) coupled to said execution switch (SCHED/ISSUE 156, see Fig. 2).

Referring to claim 7, Akkary et al. discloses as claimed an apparatus for processing; instructions in multiple threads in an execution unit (EXEC UNITS 158, see Fig. 2), comprising: an instruction buffer (instruction queue array 202A, see Fig. 10) holding a first instruction and a second instruction (see col. 9, lines 48-52, regarding instructions that are part of another thread are written into instruction queue array 202A at a different time), the first instruction being associated with a first thread, and the second instruction being associated with a second thread; a dependency counter (data and dependency array 206A see Fig. 10, and see also col. 10, lines 58-67, and col. 11, lines 1-34); an instruction control unit (control circuitry 224A, see Fig. 10) coupled to (see Fig. 10) said instruction buffer and said dependency counter, said instruction control unit (control circuitry 224A, see Fig. 10) detecting instruction dependency bits ("DEPENDENCY FIELD", see Fig. 13) and incrementing and decrementing said dependency counter ("REPLAY COUNT" see Fig. 13); and an execution switch (SCHED/ISSUE 156, see Fig. 2) coupled to (through bus 120A or 126A, see Fig. 10) said instruction control unit and said instruction buffer, said execution switch sending instructions to the execution unit (EXEC UNITS 158, see Fig. 2).

Referring to claim 12, Akkary et al. discloses as claimed an apparatus for instruction-level parallelism, comprising: an instruction buffer (instruction queue array 202A, see Fig. 10) holding a first instruction and a second instruction (see col. 9, lines 48-52, regarding instructions that are part of another thread are written into instruction queue array 202A at a different time), the first instruction being associated with a first thread, and the second instruction being associated with a second thread; and an instruction control unit (control circuitry 224A, see Fig. 10) coupled to said instruction buffer, said instruction control unit (control circuitry 224A, see Fig. 10) detecting instruction dependency bits ("DEPENDENCY FIELD", see Fig. 13) that indicate dependency between an instruction and one or more threads other than the thread with which the instruction is associated (note "DEPENDENCY FIELD" in Fig. 13 indicating the dependency between different instructions based on R1-R4 bits as shown in the figure), and sending instructions to the execution unit (EXEC UNITS 158, see Fig. 2) to be executed.

Referring to claim 23, Akkary et al. discloses as claimed a method for processing instructions in multiple threads, comprising: loading a first instruction associated with a first thread; detecting (by using control circuitry 224A, see Fig. 10)

dependency between the first instruction and a second instruction associated with a second thread based on dependency bits ("DEPENDENCY FIELD", see Fig. 13) in an instruction buffer (see col. 9, lines 48-52, regarding instructions that are part of another thread are written into instruction queue array 202A at a different time) and the value (such as "VALUE OR PRID" see Fig. 13) of a dependency counter (data and dependency array 206A see Fig. 10).

As to claim 2, Akkary et al. also discloses: the dependency counter (data and dependency array 206A see Fig. 10) includes a first counter ("REPLAY COUNT" see Fig. 13) associated with the first instruction buffer and a second counter associated with the second instruction buffer. Note as shown in Fig. 13, different "REPLAY COUNT" and "DEPENDENCY FIELD" are related to different instructions which may be saved in the first and second instruction buffers (instruction queue array 202A, see Fig. 10, see also col. 9, lines 48-52, regarding instructions are written into different trace buffer (comprising different instruction queue array 202A therein) or into instruction queue array 202A at a different time).

As to claim 3, Akkary et al. also discloses: said instruction control unit identifies instruction dependency bits ("DEPENDENCY FIELD", see Fig. 13) in said first instruction

buffer, the instruction dependency bits being associated with instructions (see Fig. 13, different "DEPENDENCY FIELD" are related to different instructions which may be saved in the first and second instruction buffers).

As to claim 4, Akkary et al. also discloses: said instruction control unit generating control signals based on the dependency bits ("DEPENDENCY FIELD", see Fig. 13) and values ("VALUE OR PRID" see Fig. 13) included in said dependency counter (data and dependency array 206A see Fig. 10, and see also col. 10, lines 58-67, and col. 11, lines 1-34).

As to claims 5 and 6, Akkary et al. also discloses: said execution switch (SCHED/ISSUE 156, see Fig. 2) providing instructions from said first instruction buffer to said execution unit (EXEC UNITS 158, see Fig. 2) based on control signals (through bus 120A or 126A, see Fig. 10) from said instruction control unit (control circuitry 224A, see Fig. 10).

As to claim 8, Akkary et al. also discloses: said dependency counter (data and dependency array 206A see Fig. 10) includes a first counter ("REPLAY COUNT" see Fig. 13) associated with the first thread and a second counter ("REPLAY COUNT" see Fig. 13) associated with the second thread (see col. 9, lines 48-52, regarding instructions that are part of another

thread are written into instruction queue array 202A at a different time).

As to claim 9, Akkary et al. also discloses: said instruction buffer includes the instruction dependency bits ("DEPENDENCY FIELD", see Fig. 13), the instruction dependency bits being associated with instructions (see Fig. 13, different "DEPENDENCY FIELD" are related to different instructions).

As to claim 10, Akkary et al. also discloses: said instruction control detects dependency between the first instruction and the second thread based on dependency bits ("DEPENDENCY FIELD", see Fig. 13) in said instruction buffer and a value (such as "VALUE OR PRID" see Fig. 13) of said dependency counter (data and dependency array 206A see Fig. 10).

As to claim 11, Akkary et al. also discloses: said first processing element (50, see Fig. 38) and said second processing element (434, see Fig. 38) are disposed within a telecommunications switch (inherently existing since a plurality of processing elements require the switch for sharing the memory see Fig. 38).

As to claim 13, Akkary et al. also discloses: said instruction control unit identifies instruction dependency bits in said instruction buffer, the instruction dependency bits being associated with the first instruction and the second

instruction (note "DEPENDENCY FIELD" in Fig. 13 indicating the dependency between different instructions based on R1-R4 bits as shown in the figure).

As to claim 14, Akkary et al. also discloses: said instruction control detects dependency between the first instruction and the second instruction based on dependency bits in said instruction buffer (note "DEPENDENCY FIELD" in Fig. 13 indicating the dependency between different instructions based on R1-R4 bits as shown in the figure).

Allowable Subject Matter

5. Claims 15-18 would be allowable if rewritten or amended to overcome the objection, set forth in this Office action.

6. Claims 19-22 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

7. Claims 24-30 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: Akkary et al., the closest reference, and the other prior art do not teach or fairly suggest:

decrementing the counter if said examining indicates that the second instruction has already been executed; and executing the first instruction (in claim 15);

incrementing a counter associated with the second thread if said determining indicates that execution of a second instruction depends on the execution of the first instruction (in claim 17); or

the instruction control unit configured to disallow execution of the first instruction if a dependency counter value is less than a threshold value (in claim 24) in combination with the other limitations of the respective independent claims and the combination is not obvious.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Kahle'233 discloses a secondary reorder buffer microprocessor comprising the issue unit used to detect the instruction dependency on

registers which are allocated on in a secondary rename registers of the secondary reorder buffer 303; Kishida et al.'112 discloses a microprocessor comprising instruction buffer 6a, 6b, instruction issue unit 2 and a counter for instruction issue control; Beard et al.'524 discloses a vector processor wherein a vector instruction may dependently initiate before a functional unit 106 or memory port is available but the vector control unit 130 will delay the first element of the vector operation until the previous operation on functional unit 106 or memory port is completed. The vector control logic 130 also provides the mechanism for chaining multiple vector instructions together. Vector control ensures that the new instruction will not get ahead of the previous instruction which is supplying it with data; and Kimura et al.'479 also discloses instruction issue control; instruction buffer and scoreboard used to show whether the resources are available or not.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

May 17, 2004